U.S.S.N. 10/632,379

Claim Amendments

Please amend claims 1, 3-6, 8, 10 - 13 and 15-20 as follows:

Listing of Claims

1. (currently amended) A field effect transistor (FET) device with enhanced performance within a decreased substrate area comprising:

a semiconductor substrate comprising an active region defined by isolation regions;

a gate electrode formed over ~~the semiconductor substrate~~ a portion of the active region and at least a portion of the isolation regions to cover and define a channel region within the ~~semiconductor substrate~~ active region; and

a pair of source/drain regions formed within the ~~semiconductor substrate~~ active region and separated by the channel region ~~within the semiconductor substrate~~, wherein said FET device further comprises at least one of:

a[[n]] corrugated interface of the active region including said channel region ~~covered by the gate electrode~~, said corrugated interface comprising rounded valley bottom portions; and

a[[n]] corrugated upper surface of the gate electrode~~, is corrugated~~.

2. (original) The field effect transistor (FET) device of claim 1 wherein the field effect transistor (FET) device is selected from the group consisting of metal oxide semiconductor field effect transistor (MOSFET) devices and metal semiconductor field effect transistor (MESFET) devices.

3. (currently amended) The field effect transistor (FET) device of claim 1 wherein the at least one of:

the corrugated interface of the ~~channel region covered by the gate electrode~~ active region; and

the corrugated upper surface of the ~~channel region covered by the~~ gate electrode, is corrugated with a peak-to-peak longitudinal periodicity of from about 0.02 to about 0.4 microns and a peak-to-valley vertical depth of from about 100 to about 1000 angstroms.

4. (currently amended) A field effect transistor (FET) device comprising:

a semiconductor substrate comprising an active region defined by isolation regions;

a gate electrode formed over ~~the semiconductor substrate~~ a portion of the active region and at least a portion of the isolation regions to cover and define a channel region within the ~~semiconductor substrate~~ active region; and

a pair of source/drain regions formed within the ~~semiconductor substrate~~ active region and separated by the channel region ~~within the semiconductor substrate~~, wherein an interface of the active region including the channel region ~~covered by the gate electrode~~ is corrugated, said corrugated interface comprising rounded valley bottom portions and peak portions.

5. (currently amended) A field effect transistor (FET) device comprising:

a semiconductor substrate comprising an active region defined by isolation regions;

a gate electrode formed over ~~the semiconductor substrate~~ a portion of the active region and at least a portion of the

isolation regions to cover and define a channel region within the ~~semiconductor substrate~~ active region; and

a pair of source/drain regions formed within the ~~semiconductor substrate~~ active region and separated by the channel region within the ~~semiconductor substrate~~ active region, wherein an upper surface of the gate electrode is corrugated, said corrugated upper surface comprising rounded valley bottom portions.

6. (currently amended) The field effect transistor (FET) device of claim 1 wherein both the interface of the ~~channel region covered by the gate electrode~~ active region and the upper surface of the gate electrode are corrugated, said corrugated interface and said corrugated upper surface comprising rounded valley bottom portions and rounded peak portions.

7. (original) The field effect transistor (FET) device of claim 1 wherein the gate electrode is formed to a thickness of from about 500 to about 2000 angstroms.

8. (currently amended) A method for forming a field effect transistor (FET) device comprising:

providing a semiconductor substrate comprising an active region defined by isolation regions;

forming a gate electrode over ~~the semiconductor substrate~~ a portion of the active region and at least a portion of the isolation regions to cover and define a channel region within the ~~semiconductor substrate~~ active region ~~a gate electrode~~; and

forming within the ~~semiconductor substrate~~ active region and separated by the channel region within the ~~semiconductor substrate~~ active region a pair of source/drain regions, wherein said FET device further comprises at least one of:

a[[n]] corrugated interface of the active region including said channel region ~~covered by the gate electrode~~, said corrugated interface comprising rounded valley bottom portions; and

a[[n]] corrugated upper surface of the gate electrode~~, is corrugated~~.

9. (original) The method of claim 8 wherein the field effect transistor (FET) device is selected from the group consisting of metal oxide semiconductor field effect transistor (MOSFET)

devices and metal semiconductor field effect transistor (MESFET) devices.

10. (currently amended) The method of claim 8 wherein the at least one of:

the corrugated interface of the ~~channel region covered by the gate electrode~~ active region; and

the corrugated upper surface of the gate electrode, is corrugated with a peak-to-peak longitudinal periodicity of from about 0.02 to about 0.4 microns and a peak-to-valley vertical depth of from about 100 to about 1000 angstroms.

11. (currently amended) A method for forming a field effect transistor (FET) device comprising:

providing a semiconductor substrate comprising an active region defined by isolation regions;

forming a gate electrode over ~~the semiconductor substrate~~ a portion of the active region and at least a portion of the isolation regions to cover and define a channel region within the ~~semiconductor substrate~~ active region ~~a gate electrode~~; and

forming a pair of source/drain regions within the ~~semiconductor substrate~~ active region and separated by the channel region within the ~~semiconductor substrate~~ active region ~~a pair of source/drain regions,~~ wherein an interface of the ~~channel region covered by the gate~~ active region is corrugated, said corrugated interface comprising rounded valley bottom portions and peak portions.

12. (currently amended) A method for forming a field effect transistor (FET) device comprising:

providing a semiconductor substrate comprising an active region defined by isolation regions;

forming a gate electrode over ~~the semiconductor substrate~~ a portion of the active region and at least a portion of the isolation regions to cover and define a channel region within the ~~semiconductor substrate~~ active region ~~a gate electrode~~; and

forming a pair of source/drain regions within the ~~semiconductor substrate~~ active region and separated by the channel region within the ~~semiconductor substrate~~ active region ~~a pair of source/drain regions,~~ wherein an upper surface of the gate electrode is corrugated, said corrugated surface comprising

rounded valley bottom portions.

13. (currently amended) The method of claim 8 wherein both the interface of the active region ~~channel region covered by the gate electrode~~ and the upper surface of the gate electrode are corrugated, said corrugated interface and said corrugated upper surface comprising rounded valley bottom portions and rounded peak portions.

14. (previously presented) The method of claim 8 wherein the gate electrode is formed to a thickness of from about 500 to about 2000 angstroms.

15. (previously presented) The field effect transistor (FET) device of claim 1 wherein the ~~semiconductor substrate comprises materials selected from the group consisting of~~ corrugated interface comprises silicon ~~and compound semiconductors~~.

16. (previously presented) The field effect transistor (FET) device of claim 4 wherein the ~~semiconductor substrate comprises materials selected from the group consisting of~~ corrugated interface comprises silicon ~~and compound semiconductors~~.

17. (previously presented) The field effect transistor (FET)

device of claim 5 wherein the ~~semiconductor substrate comprises materials selected from the group consisting of~~ corrugated interface comprises silicon ~~and compound semiconductors~~.

18. (previously presented) The method of claim 8 wherein the ~~semiconductor substrate comprises materials selected from the group consisting of~~ active region comprises silicon ~~and compound semiconductors~~ and the corrugated interface is formed by a method selected from the group consisting of oxidation and etching.

19. (previously presented) The method of claim 11 wherein the ~~semiconductor substrate comprises materials selected from the group consisting of~~ active region comprises silicon ~~and compound semiconductors~~ and the corrugated surface is formed by is formed by a method selected from the group consisting of oxidation and etching.

20. (previously presented) The method of claim 12 wherein the ~~semiconductor substrate comprises materials selected from the group consisting of~~ active region comprises silicon ~~and compound semiconductors~~ and the corrugated surface is formed by a method selected from the group consisting of oxidation and etching.